

## CLAIMS

1. A target formed on a substrate comprising:  
a first layer deposited below a second layer on the substrate, the second layer deposited below a third layer on the substrate, the first layer having the  
5 topographic contour formed thereon, the first layer at least partially projecting a patterned topographical contour through the second layer to the third layer.
2. The target as set forth in claim 1, wherein the optical characteristic of the patterned topographical contour of the first layer differs from the optical characteristics of portions of the first layer surrounding the patterned  
10 topographical contour.
3. The target as set forth in claim 1, wherein the optical characteristic of the patterned topographical contour of the third layer differs from the optical characteristics of portions of the third layer surrounding the patterned topographical contour.
- 15 4. The target as set forth in claim 1, wherein the patterned topographical contour includes a plurality of alternating relatively brighter and relatively darker sections.
5. The target as set forth in claim 1, wherein the patterned topographical contour include a plurality of alternating conductors and insulators.
- 20 6. The target as set forth in claim 1, wherein the patterned topographical contour of the third layer results from a configuration of polysilicon in the first layer.

7. The target as set forth in claim 1, wherein a die includes the substrate, wherein the first layer and the second layer are deposited on at least a portion of the die.
8. The target as set forth in claim 7, wherein a width of the die is less than  
5 or equal to 5 mm.
9. The target as set forth in claim 1, wherein the topographic portion includes a plurality of indentations that are arranged in a grid pattern.
10. The target as set forth in claim 1, wherein the first layer is an electrical conductor, the second layer is an electrical insulator, and the third layer is an  
10 electrical conductor.
11. The target as set forth in claim 1, wherein the second layer includes an electrical conductor.
12. The target as set forth in claim 1, wherein electrical current flows through at least one of the first layer and the third layer.
- 15 13. The target as set forth in claim 1, wherein the substrate is segmented into at least one electrically functional portion and at least one electrically non-functional portion.
14. The target as set forth in claim 13, wherein the target is at least partially located on the electrically functional portion.
- 20 15. The target as set forth in claim 1, further comprising a transparent layer deposited above the patterned topographical contour.

16. The target as set forth in claim 1, wherein at least a portion of the third layer is recessed.

17. The target as set forth in claim 1, wherein the topography of two portions of an upper surface of the topographic portion are at different vertical heights.

18. The target as set forth in claim 1, wherein the topography of the upper surface includes a central region, and a contrasting region located around the central region.

19. The target as set forth in claim 18, wherein the contrasting region includes a pattern that is at least partially determined by the topographical contour.

20. The target as set forth in claim 1, wherein at least a portion of the second and third layers are transparent.

21. The target as set forth in claim 1, further comprising:  
a barrier layer disposed above the second layer; and  
an orifice plate disposed above the barrier layer.

22. The target as set forth in claim 21, wherein the target is an orifice alignment target.

23. A method of manufacture of a target, comprising:  
depositing a first layer on a substrate;  
forming a topographic portion on an upper surface of the first layer; and  
depositing a second layer on the substrate, wherein the topographic portion is projected through the second layer to form a patterned topographical

contour on an upper surface of the second layer, wherein the patterned topographical contour acts as at least a portion of the target.

24. The method as set forth in claim 23, wherein the forming the first layer includes patterning substantially in parallel strips; the parallel strips including  
5 alternating strips of relatively bright light and relatively dark light when direct light is applied at the target.

25. The method as set forth in claim 23, wherein the forming the first layer includes patterning substantially in parallel strips, the parallel stripes including alternating strips of relatively bright light and relatively dark light when  
10 indirect light is applied at the target.

26. The method as set forth in claim 23, wherein the forming the first layer includes indentations formed in the first layer, the indentations are arranged in a grid pattern.

27. A method of using an electrically-functional optical target located on an  
15 integrated circuit, the target having a patterned topographical contour located on a second layer that is projected from a topographical contour formed on a first layer, the method comprising:

directing light at the target to optically determine the location of the target; and

20 passing an electric current through the target in the first layer, wherein the electric current at least partially passes from a first portion of the integrated circuit outside of the target, through the first layer within the target, and to a second portion of the integrated circuit outside of the target.

**28.** The method as set forth in claim 27, wherein the integrated circuit is integrated in a printhead.

**29.** A method of locating an optical target on a die, the method comprising:  
illuminating the die with light;

5 reflecting the light toward an observation position from one portion of the target and away from the observation position from another portion of the target;

sensing the reflected light off the die as the optical target based on relatively brighter areas and darker areas that is reflected toward the

10 observation position.

**30.** The method of claim 29, wherein the light that is illuminating certain portions of the die is direct light.

**31.** The method of claim 29, wherein the light that is illuminating certain portions of the die is indirect light.

15 **32.** The method of claim 29, wherein the die is integrated in a printhead.

**33.** The method of claim 29, further comprising a wafer that includes at least one die.

20 **34.** An alignment target, comprising:  
an arrangement of layers disposed on a substrate so as to form a region of optical contrast, the arrangement including

at least one electrically conductive layer adapted to conduct current therethrough.

**35.** The alignment target of claim 34, the arrangement further comprising:  
at least one electrically insulative layer adapted to inhibit the conduction  
of current therethrough.

5 **36.** The alignment target of claim 35, wherein the at least one electrically  
conductive layer is a plurality of electrically conductive layers, and wherein at  
least one of the insulative layers is disposed between a pair of the conductive  
layers.

**37.** The alignment target of claim 36, wherein at least one of the insulative  
10 layers is disposed between each adjacent pair of the conductive layers.

**38.** The alignment target of claim 34, wherein the alignment target has an  
optical boundary, and wherein at least one of the electrically conductive layers  
extends beyond the optical boundary.

**39.** The alignment target of claim 34, wherein the at least one electrically conductive layer forms a portion of an electrical circuit.

**40.** The alignment target of claim 39, wherein the electrical circuit is disposed on the substrate.

5 **41.** The alignment target of claim 34, wherein the layers include thin film layers.

**42.** The alignment target of claim 34, wherein the thin film layers are fabricated using a semiconductor technology selected from the group of metal-oxide semiconductor, metal-oxide semiconductor field effect transistor, metal-  
10 insulator semiconductor, and combined metal-oxide semiconductor technology.

**43.** The alignment target of claim 34, the arrangement further comprising: at least one semiconductor layer.

**44.** The alignment target of claim 34, wherein the region of optical contrast comprises:  
15 a sloped portion angled with respect to a surface of the substrate.

**45.** The alignment target of claim 34, wherein at least one layer of the arrangement includes a topographical pattern portion.

**46.** A printhead including the alignment target of claim 34.